

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Tsuyoshi ONO; Yasuaki HIRANO; Masahiko WATANABE; and Sau Ching WONG

Application No: NEW

Filed: January 21, 2004

For: NONVOLATILE SEMICONDUCTOR MEMORY DEVICE

INFORMATION DISCLOSURE STATEMENT
(SUBMISSION CONCURRENT WITH THE
FILING OF A NEW PATENT APPLICATION)

January 21, 2004

MAIL STOP NEW APPLICATION
COMMISSIONER FOR PATENTS
P.O. BOX 1450
Alexandria, Virginia 22313-1450

Sir:

Pursuant to 37 C.F.R. §§ 1.97 and 1.98, applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on PTO-1449, attached hereto.

II. COPIES

☒ Submitted herewith is a legible copy of (i) each foreign patent; (ii) each publication or that portion which caused it to be listed; and (iii) all other information or that portion which caused it to be listed.

☐ This application is a National Phase of a PCT application. Some or all of the documents listed on the PTO-1449 are not enclosed because they were cited in the International Search Report and copies should be forwarded from the International Search Authority. If copies are needed, please contact the undersigned.

- ☐ Because the present application is being filed after June 30, 2003, no copies of the U.S. patents or U.S. patent application publications which are listed on the attached Form 1449 are enclosed pursuant to the waiver of 37 C.F.R. § 1.98(a)(2)(i). Any foreign patent documents or non-patent literature listed on the attached Form 1449 are enclosed herewith.

III. CONCISE EXPLANATION OF THE RELEVANCE
(check at least one box)

a. ☒ **DOCUMENTS IN THE ENGLISH LANGUAGE**

The attached patents, publications, or other information in the English language do not require a statement of relevancy.

b. ☒ **DOCUMENTS NOT IN THE ENGLISH LANGUAGE**

A concise explanation of the relevance of all patents, publications, or other information listed that is not in the English language is as follows:

The publications use the technique of increasing the gate voltage by ΔV_{pp} , wherein the program to be used has a constant programming pulse width in a programming algorithm for matching V_t of one state. In this case, if distribution of the V_t is required to be narrowed for the purpose of realizing high-speed flash memory of multilevel, "over-programming" is easy to occur.

A partial English translation has been provided for the Japanese Patent No. JP 11-134879.

c. ☐ **OTHER**

For the Examiner's convenience, we attach hereto U.S. Patent No. , which is the corresponding U.S. equivalent of . Submission of the English language equivalent(s) is deemed to satisfy the requirement for a concise explanation of relevancy.

FEES

This Information Disclosure Statement is being filed concurrently with the filing of a new patent application; therefore, no fee is required.

If The Examiner has any questions concerning this IDS, he/she is requested to contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the PTO is requested to consider this IDS under the proper rule and charge the appropriate fee to Deposit Account No. 08-0750.

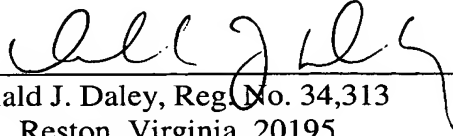
New U.S. Application
Docket No. 1768-000001/US

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKY & PIERCE, P.L.C

By: _____


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DJD:jj

Enclosures: ☒ Form PTO-1449(s)
☒ Documents
☐ Fee

Form PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION (Use several sheets if necessary)				ATTY DOCKET NO. 1768-000001/US		APPLICATION NO.	
				APPLICANT Tsuyoshi ONO, et al.		CONF. NO. Unknown	
				FILING DATE January 21, 2004		GROUP Unknown	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE	
FOREIGN PATENT DOCUMENTS							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION	
						YES	NO
	JP 11-134879	5/21/1999	JAPAN			ABST.	
OTHER DOCUMENTS (Include Name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.							
		Giovanni Campardo, et al., "40-mm2 3-V-Only 50-MHz 64-Mb 2-v/Cell CHE NOR Flash Memory", IEEE Journal Of Solid-State Circuits, Vol. 35, No. 11, November 2000					
EXAMINER				DATE CONSIDERED			
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

DJD:jj